PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Alan R. Reinberg

Serial No.: 09/189,098

Filed: November 9, 1998

For: WEAK THERMAL/ELETRICAL LINK FOR VERTICALLY CONTACTED STRUCTURES

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in TRIPLICATE pursuant to 37 C.F.R. § 1.192(a) in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

U.S. Serial No. 09/189,098 (hereinafter "the '098 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. ("Assignee"). The assignment has been recorded with the United States Patent & Trademark Office ("Office") at Reel No. 9582, Frame No. 0907. Accordingly, Micron Technology, Inc. is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant nor the undersigned attorney is currently aware of any appeals or interference proceedings that would affect or be affected by the Board's decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

Claims 1-20 and 32-71 remain pending and under consideration in the '098 Application. Each of these claims stands rejected.

Claims 21-31 have been canceled from the '098 Application without prejudice or disclaimer.

No claims have been allowed.

The rejections of claims 1-20 and 32-71are being appealed.

(4) STATUS OF AMENDMENTS

The above-referenced application was originally filed with 67 claims.

On March 28, 2000, a restriction requirement was made in the '098 Application.

A response to the restriction requirement, which was filed on April 10, 2000, included an election, without traverse, to prosecute claims 1-20 and 32-67.

A Preliminary Amendment was filed on May 11, 2000.

On June 20, 2000, a first Office Action on the merits was issued. All of the claims that remained under consideration in the '098 Application were rejected in that Office Action.

An Amendment was filed on September 20, 2000, in response to the first Office Action. In the Amendment claims 21-31, which had been withdrawn from consideration pursuant to the restriction requirement, were canceled without prejudice or disclaimer. In addition, several claim amendments were presented, as were explanations as to the allowability of each of the claims that remained under consideration.

All of the claims were again rejected in a second, final Office Action, dated December 5, 2000.

In response, an Amendment Under 37 C.F.R. § 1.116 was filed on January 31, 2001. Further claim amendments and explanations were provided in that Amendment.

In an Advisory Action dated February 12, 2001, it was indicated that the claim amendments would require a further search and, thus, would not be entered unless a Continued Prosecution Application or Request for Continued Examination were filed.

A Request for Continued Examination and another Amendment were filed on February 21, 2001. In that Amendment, new claims 69-73 were added.

A third Office Action was issued on May 14, 2001. Again, each of claims 1-20 and 32-71 stood rejected.

A response to the third Office Action was filed on August 17, 2001, in which further explanations were provided as to why each of claims 1-20 and 32-71 was allowable over the art on which the Office was relying in its rejections.

On October 24, 2001, a fourth, final Office Action was mailed. The prior art rejections of claims 1-20 and 32-71 were maintained.

Thereafter, on December 20, 2001, another Amendment Under 37 C.F.R. § 1.116 was filed.

Evidently, the Office lost that Amendment. Following an inquiry as to the status of the '098 Application, another copy of the December 20, 2001, Amendment was provided to the Office.

In an Advisory Action that was mailed on May 29, 2002, all of the claims were again rejected. In addition, pursuant to applicant's request, the Office sent a Notice of Abandonment on May 29, 2002.

A Petition to Revive was filed, along with another Request for Continued Examination and the appropriate fees, on June 14, 2002.

A Decision that was mailed on August 20, 2002, indicates that the petition was granted.

On October 21, 2002, a fifth Office Action was mailed. The prior art rejections of claims 1-20 and 32-71 were again asserted.

Another responsive Amendment was filed on January 27, 2003, in which further claim arguments were presented, as was further reasoning as to the allowability of the claims. After that Amendment, no further claim amendments were presented in the '098 Application.

On March 12, 2003, a sixth, final Office Action followed. The Office finally revised its prior art rejections of the claims, but continued to reject each of claims 1-20 and 32-71 nonetheless.

In another attempt to convince the Office of the patentability of claims 1-20 and 32-71, a Response to Final Office Action was filed on May 16, 2003.

Unfortunately, the Office did not allow any of claims 1-20 and 32-71, maintaining each of its rejections in an Advisory Action dated May 27, 2003.

On May 12, 2003, a Notice of Appeal was mailed, and is followed by this Appeal Brief.

(5) SUMMARY OF THE INVENTION

The '098 Application describes and includes claims that are drawn to electrical contacts. An electrical contact 10 of the type disclosed in the '098 Application includes an intermediate conductive layer 16, an insulator component 20 positioned adjacent to the intermediate conductive layer 16, and an electrically conductive contact layer 22 positioned adjacent to the insulator component 20 and in communication with the intermediate conductive layer 16. FIG. 2; page 7, line 26, to page 8, line 3. The intermediate conductive layer 16 contacts and is in electrical communication with a structure 12 which is located at a lower level of a semiconductor device of which the contact 10 is a part than a silicon-containing dielectric layer 11 of the semiconductor device. FIG. 2. The intermediate conductive layer 16 and the conductive contact layer 22 may substantially envelop the insulator component 20. FIG. 2; page 7, line 26, to page 8, line 3. In such a configuration, the conductive layers 16, 22 of the contact 10 may facilitate electrical communication between the contacted structure 12 and circuit elements which

are external to the semiconductor device, while the insulator component 20 may thermally insulate the contacted structure 12. FIG. 2; page 8, lines 27 & 28.

As an example, the structure 12 that is contacted by the contact of the '098 Application may comprise a memory element 32, such as an electrically-erasable, programmable (EEPROM) memory element. FIG. 9; page 12, line 27, to page 13, line 3. An example of an EEPROM memory element that may be contacted is a so-called "phase change" element 13, which has at least two different conductivity states that depend upon the temperature of a "phase change" material thereof. FIG. 9; page 8, lines 4-10; page 13, lines 4, 5, and 20-24. The insulator component 20 of the contact 10 may beneficially facilitate maintenance of a desired temperature of such a phase change component 13. Page 13, line 24, to page 14, line 2.

(6) ISSUES

(A) Whether, under 35 U.S.C. § 103(a), claims 1-6, 8-10, 32-38, and 68-70 are nonobvious and, thus, allowable over the combination of teachings from U.S. Patent 5,792,594 to Brown et al. (hereinafter "Brown"), in view of the teachings of U.S. Patent 4,770,977 to Buiguez et al. (hereinafter "Buiguez");

(B) Whether, under 35 U.S.C. § 103(a), claim 11 is nonobvious and, thus, allowable over the teachings of Brown, in view of the teachings of Buiguez and, further, in view of teachings from U.S. Patent 5,451,811 to Whitten et al. (hereinafter "Whitten");

(C) Whether, under 35 U.S.C. § 103(a), claims 7, 12-19, 39-54, 56-66, 69, and 71 are nonobvious and, thus, allowable over the teachings of U.S. Patent 5,296,719 to Ovshinsky et al. (hereinafter "Ovshinsky"), in view of the teachings of Brown and Buiguez; and

(D) Whether, under 35 U.S.C. § 103(a), claims 20, 55, and 67 are nonobvious and, thus, allowable over the combined teachings of Ovshinsky, Brown, Buiguez, and Whitten.

(7) GROUPING OF CLAIMS

Group 1 – Claims 1-11, 32-38, and 68-71:

Claims 1-11, 32-38, and 68-71 should be grouped together. Claim 1 is the most generic claim of Group 1. Each of claims 2-11, 32-38, and 68-71 stand with claim 1. Claims 7, 10, 11, 68, and 70 do not, however, fall with claim 1.

Group 2 – Claims 12-20:

Claims 12-20 should be grouped together. Claim 12 is the most generic claim of this group. Claims 13-20 stand with claim 12, but claim 20 does not fall with claim 12.

Group 3 – Claims 39-67:

Claims 39-67 should be grouped together. Of these, claim 56 appears to be the most generic. While claims 39-55 and 57-67 stand with claim 45, claims 55 and 67 do not fall with claim 45.

(8) ARGUMENT

Claims 1-20 and 32-71 stand rejected under 35 U.S.C. § 103(a).

(A) Applicable Law

The standard for a claim rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(B) References Relied Upon

Brown

Brown teaches a method for repatterning semiconductor dice for use in flip-chip applications, as well as various products of the method. The method taught in Brown includes forming a first dielectric polymer layer on a dielectric layer of a semiconductor die that laterally surrounds and is located in the same plane as bond pads of the semiconductor die. Col. 3, lines 3-7. The bond pads are then exposed through the first dielectric polymer layer. Col. 3, lines 7 & 8. Next, a second dielectric polymer layer is formed over the first dielectric polymer layer (col. 3, lines 8-12), and the bond pads and areas of the first dielectric polymer layer upon which circuit traces are to be carried through the second dielectric polymer layer are exposed through the second dielectric polymer layer (col. 3, lines 12-15).

The first dielectric polymer layer used in the method that is taught in Brown includes a catalyst. Col. 3, lines 3-7. A catalytic metal is also deposited onto the exposed bond pad. Col. 3, lines 15-18. The catalyst of the first dielectric polymer layer and the catalytic metal of the

exposed bond pad facilitate copper plating of the first dielectric polymer layer and of the bond pad. Col. 3, lines 21-24. The exposed portion of each bond pad and the exposed portions of the first dielectric polymer layer are then plated with a metal, such as copper, that has better conductivity properties and is less corrosive than aluminum. Col. 3, lines 24-28. Upon patterning the metal plating, conductive lines and contact pads are formed. Col. 3, lines 28-31.

In one described example of the resulting semiconductor die, which is shown in FIG. 4, the new contact pad is formed directly above the corresponding bond pad 12 and is separated from the active surface of the semiconductor die by the two dielectric polymer layers 14, 18. The bond pad 12 is depicted as being located at the same level as and laterally surrounded by a dielectric layer 11, which may be formed from a variety of silicon-containing materials, such as silicon nitride, silicon dioxide, or a glassified surface. As depicted, neither the upper, copper layer 26 or the lower, nickel layer 22 of the new contact pad contacts the silicon-containing dielectric layer 11.

Brown does not teach or suggest that the formed structure is useful for anything other than to produce a precision interconnecting pattern and terminal bump pattern from metals other than aluminum so as to enhance the performance of a semiconductor die. Col. 2, lines 46-49 and 55-57.

Buiguez

Buiguez teaches silicon-containing polymers that are useful as photomasks in lithography (*i.e.*, etching) processes.

Whitten

The portion of Whitten that has been relied upon in the rejections that have been presented in the '098 Application is drawn to an embedded upper electrode of an antifuse.

Ovshinsky

Ovshinsky teaches an electrically erasable programmable memory (EEPROM) that includes memory elements formed from a phase change material. Col. 5, lines 14-20. The phase change material has a plurality of electrical conductivity states, depending upon whether the material is in an amorphous state, a crystalline state, or an intermediate state. Col. 5, lines 28-38. The state of the material depends upon the amount of energy (*e.g.*, heat) applied to the memory element. *Id.* Ovshinsky does not recognize heat loss as a problem or disclose contacts or other structures to at least thermally insulate the phase change memory elements of the EEPROM disclosed therein.

(C) Rejections Presented

(i) Brown and Buiguez

Claims 1-6, 8-10, 32-38, and 68-70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Brown, in view of the subject matter taught in Buiguez.

Of these rejected claims, claims 1 and 32 are independent.

Independent claim 1 of the '098 Application recites a contact that includes an intermediate conductive layer, an insulator component positioned "so as to at least thermally insulate [a] structure" of the semiconductor device, and an electrically conductive contact layer.

The intermediate conductive layer of independent claim 1 contacts and is in electrical communication with *the structure*, which *is located at a lower level than* a silicon-containing dielectric layer of the semiconductor device.

Independent claim 32 recites, among other things, a contact that includes "a contact layer and an intermediate conductive layer which partially contact one another and substantially envelop an insulator component . . ." The contact "contacting a structure located *at a lower level than* a silicon-containing dielectric layer of the semiconductor device so as to at least thermally insulate underlying structure." (Emphasis supplied).

It is respectfully submitted that there are several reasons that a *prima facie* case of obviousness has not been established against any of claims 1-6, 8-10, 32-38, or 68-70.

No Motivation to Combine

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Brown and Buiguez in the manner that has been asserted. In particular, while Buiguez teaches a silicon-containing polymer that is useful as a photomask on intermediate semiconductor device structures, neither Buiguez nor Brown provides any suggestion or motivation to one of ordinary skill in the art to use that silicon-containing polymer for any other purpose; namely, for a dielectric layer which resides at a higher level of a semiconductor device than a structure which is contacted by a contact of the semiconductor device.

Further, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by Brown, Buiguez, or the knowledge that was generally available in the art before the filing date of the above-referenced application to combine the teachings of Brown and Buiguez in the manner that has been asserted to render the subject matter recited in claims 68 and 70 unpatentable. Specifically, the copper conductive portions of the contact of Brown could not contact a silicon-containing structure, such as the silicon-containing polymer of Buiguez, since, as is well known to those of skill in the art, copper reacts with silicon-containing materials in a manner that causes the copper to blister or delaminate from adjacent silicon-containing structures. The teachings of Brown are not inconsistent with these well-known facts. FIG. 4 of Brown illustrates a copper layer 26 that does not contact an proximate silicon-containing layer 11, but is instead separated therefrom by way of a resin layer 14.

It therefore appears that any motivation to combine the teachings of Brown and Buiguez in the manner that has been asserted could only have been improperly gleaned from the disclosure of the above-referenced application.

For these reasons, it appears that the asserted combination of teachings from Brown and Buiguez could only have been based upon the benefit of hindsight provided by the subject matter disclosed and recited in the claims of the above-referenced patent application.

Therefore, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established against any of claims 1-6, 8-10, 32-38, or 68-70.

There Is No Reason to Expect the Asserted Combination to Be Successful

With respect to dependent claims 68 and 70, it is also respectfully submitted that, because a copper contact cannot abut a silicon-containing protective layer without resulting in blistering or delamination of the copper contact from the protective layer, there would have been no reason for one of ordinary skill in the art to expect that combining the teachings of Brown and Buiguez in the asserted manner would have been successful.

Thus, the Office has not established a *prima facie* case of obviousness against any of claims 1-6, 8-10, 32-38, or 68-70.

Brown and Buiguez Do Not Teach or Suggest Each and Every Claim Element

It is also respectfully submitted that, even when the teachings of Brown and Buiguez are combined in the manner that has been asserted, Brown and Buiguez do not teach or suggest each and every element of any of claims 1-6, 8-10, 32-38, or 68-70.

With respect to the subject matter recited in independent claim 1, while it is acknowledged that Brown, at col. 4, lines 63-67, teaches that "pads 12 . . . may be located anywhere in an integrated circuit . . .," this blanket statement does not amount to a teaching or suggestion by Brown of pads 12 that are located at a lower level of a semiconductor device than the silicon-containing dielectric layer 11 thereof. Rather, the relevant teachings of Brown, as shown in FIG. 4 thereof, are limited to a semiconductor device structure that includes a contact that is positioned adjacent to a pad 12 which itself is located at the *same level* of the semiconductor device as that in which the dielectric layer 11 thereof is located. Thus, Brown does not teach or suggest a contact that contacts a structure located *at a lower level than* a

silicon-containing dielectric layer of semiconductor device, as is recited in claim 1, as proposed to be amended.

Buiguez likewise lacks any teaching or suggestion that the silicon-containing polymer taught therein may be used on a semiconductor device at a higher level thereof than a structure which is contacted by a contact of the semiconductor device. Instead, the teachings of Buiguez are limited to using the polymer as a photomask in photolithography processes and, thus, to semiconductor device structures which are still under fabrication and do not yet include contacts, let alone contacts of the type recited in independent claim 1.

Further, Buiguez does not include any teaching or suggestion that the silicon-containing polymers described therein may remain within semiconductor devices. Rather, as is well-known in the art, photomasks are typically removed from semiconductor device structures and, therefore, would not ordinarily remain in place over a structure which is contacted by a contact.

Moreover, Brown and Buiguez both lack any teaching, suggestion, or express or inherent description that the insulator component of the contact thereof may be positioned so as to thermally insulate an underlying structure of the semiconductor device.

Therefore, Brown and Buiguez, taken either alone or together, do not teach or suggest each and every element of independent claim 1.

Claims 2-6, 8-10, and 68 are each allowable, among other reasons, as depending from claim 1, which is allowable.

In addition, claim 10 is allowable since Brown and Buiguez both lack any teaching or suggestion of a contact that includes a contact layer comprising "a material having a melting temperature that is greater than a temperature required to switch a phase change component in

electrical communication with the contact between a plurality of states." In fact, Brown does not teach, suggest, or expressly or inherently describe that the contact disclosed therein may be positioned adjacent to a structure that includes a phase change component or that the semiconductor device disclosed therein could even include a phase change component.

Claim 68 is additionally allowable since neither Brown nor Buiguez teaches or suggests that an intermediate conductive layer or an electrically conductive contact layer of the contact described therein may abut a silicon-containing structure. Rather, Brown merely teaches that the copper contacts thereof are in contact with a photodefinable resin layer.

As for independent claim 32 it is understood that, as a product-by-process claim, the only limitations considered by the Office in determining patentability thereof are the product limitations. It is respectfully submitted that neither Brown nor Buiguez teaches or suggests a contact that contacts a structure located *at a lower level than* a silicon-containing dielectric layer of a semiconductor device. Rather, the teachings and suggestions of Brown are limited to a contact that contacts a pad 12 which is located at the same level as a silicon-containing dielectric layer 11 of a semiconductor device and to contacts that are laterally offset from other structures of the semiconductor device. The mere statement at col. 4, lines 63-67, of Brown that pads 12 may be located "anywhere" does not amount to a teaching or suggestion of anything other than the embodiments that have been described therein with any amount of detail.

Buiguez lacks any teaching or suggestion that the silicon-containing polymer described therein may be used for any purpose other than as a photomask.

Further, Brown and Buiguez both fail to teach or suggest a contact that may be positioned so as to at least thermally insulate a contacted structure.

Therefore, Brown does not teach or suggest each and every element of independent claim 32, as required to maintain a rejection under 35 U.S.C. § 103(a). Accordingly, under 35 U.S.C. § 103(a), independent claim 32 is allowable over Brown.

Each of claims 33-38 and 70 is allowable, among other reasons, as depending from claim 32, which is allowable.

Claim 70 is additionally allowable since Brown and Buiguez both lack any teaching or suggestion of a contact with either an intermediate conductive layer or an electrically conductive contact layer that abuts a major surface of a silicon-containing dielectric layer of a semiconductor device. Rather, FIG. 4 of Brown illustrates that the copper layer 26 of the contact thereof only abuts an upper surface of resin layer 18, an edge of resin layer 14, and an upper surface of pad 12.

In view of the foregoing, reversal of the 35 U.S.C. § 103(a) rejections of claims 1-6, 8-10, 32-38, 68, and 70 is respectfully solicited.

(ii) Brown in View of Buiguez and Whitten

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Brown, in view of teachings from Buiguez and Whitten.

Claim 11 is allowable, among other reasons, as depending from independent claim 1, which is allowable.

In addition, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by Brown, Buiguez, Whitten, or the knowledge that was generally available in the art to combine the teachings of Brown and Whitten in the asserted manner. Specifically, Brown teaches an *external* contact for a semiconductor device, while the portion of Whitten that is relied upon is drawn to an *embedded* and, thus, buried

upper electrode of an antifuse. Buiguez's teaching of silicon-containing photoresist materials does not bridge the diversity between the teachings of Brown and Whitten.

For these reasons, it is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been set forth and requested that the 35 U.S.C. § 103(a) rejection of claim 11 be reversed.

(iii) Ovshinsky in View of Brown and Buiguez

Claims 7, 12-19, 39-54, 56-66, 69, and 71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the subject matter taught in Ovshinsky, in view of the teachings of Brown and Buiguez.

It is respectfully submitted that there are several reasons that a *prima facie* case of obviousness has not been set forth, as is required to maintain a rejection under 35 U.S.C. § 103(a).

Independent claim 12 recites a contact for a memory element that includes a phase change component. The contact includes, among other things, an intermediate conductive layer adjacent to and in electrical and thermal communication with the memory element.

Independent claim 39 recites an electrically erasable programmable memory device that includes, among other things, a memory element and a contact. The memory element includes at least one of an electrode and a memory cell that comprises a phase change material. The contact includes, among other things, an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with the memory element, as well as an insulator component adjacent the intermediate conductive layer.

Independent claim 45 recites a semiconductor device that includes at least one contact with, among other things, an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with a structure of the semiconductor device that comprises a phase change component.

Independent claim 56 recites an enhanced electrically erasable programmable element with a contact that includes "an intermediate conductive layer positioned adjacent to and in electrical communication with the electrically erasable programmable element; an insulator component disposed adjacent said intermediate conductive layer and over the electrically erasable programmable element so as to insulate same; and an electrically conductive contact layer adjacent said insulator component."

Claim Dependency

First, it is respectfully submitted that claim 7 is allowable, among other reasons, as depending from claim 1, which is allowable.

No Motivation to Combine

Second, it is respectfully submitted that one of ordinary skill in the art, prior to the time at which the referenced application was filed, would not have been motivated to combine the teachings of Ovshinsky, Brown, and Buiguez in the manner that has been asserted. Specifically, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine a memory element, an electrically erasable programmable element, or any other structure that includes a phase change component with a contact including an intermediate conductive layer, an insulator component, and a contact layer, with the intermediate conductive layer of the contact being positioned adjacent to and in electrical or thermal communication with the memory element or other structure, as is recited in independent claims 12, 39, 45, and 56.

While FIG. 4 of Brown depicts a conductive terminal positioned above a corresponding bond pad formed from a different conductive material, and the structure has a similar appearance to that shown in the figures of the referenced application, Brown does not provide any suggestion or motivation that the structure illustrated in FIG. 4 could be used adjacent a memory cell or other structure similar in type to that taught in Ovshinsky.

Furthermore, Ovshinsky, which discloses an EEPROM that includes phase change elements, would also have failed, prior to the time at which the referenced application was filed, to have provided any suggestion or motivation to one of ordinary skill in the art to dispose a contact of a type recited in the claims of the referenced application adjacent to a memory cell or other structure including a phase change component in such a manner that would thermally insulate the phase change element. In fact, Ovshinsky does not even recognize a need for thermally insulating the phase change elements of the EEPROM disclosed therein. Moreover,

the figures of Ovshinsky do not depict discrete electrical contacts, such as the exposed contacts of Brown, in communication with each memory element, but rather an encapsulated conductive line that connects adjacent memory elements.

As Buiguez merely teaches silicon-containing photoresists, it could not provide any suggestion or motivation which makes up for the deficiencies of Ovshinsky and Brown.

It is further submitted that the knowledge generally available in the art prior to the time the present application was filed would also have failed to provide one of ordinary skill in the art with any suggestion or motivation to combine the teachings of Ovshinsky with the teachings of Brown or Buiguez.

Accordingly, it is respectfully submitted that any motivation to one of ordinary skill in the art to combine the teachings of Ovshinsky, Brown, and Buiguez could only be improperly based on the hindsight provided by the disclosure and claims of the referenced application.

As there would not have been any motivation for one of ordinary skill in the art to combine the teachings of Ovshinsky, Brown, and Buiguez in the manner that has been asserted, it is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established.

The Asserted Combination of References Do Not Teach or Suggest Each and Every Claim Element

Third, it is respectfully submitted that Ovshinsky, Brown, and Buiguez do not, taken either together or separately, teach or suggest each and every element of any of claims 12-19, 39-54, 56-66, 69, or 71.

Again, independent claim 12 recites a contact for a memory element that includes a phase change component. The contact includes, among other things, an intermediate conductive layer adjacent to and in electrical and thermal communication with the memory element.

None of Ovshinsky, Brown, or Buiguez, taken alone or in combination, teaches or suggests a contact for a memory element, which contact includes an intermediate conductive layer adjacent to and *in electrical and thermal communication with the memory element*. Rather, Brown teaches a contact pad that is located adjacent to a bond pad. Ovshinsky teaches adjacent memory elements that are bridged, or electrically connected, to one another by way of an upper conductor 42. The upper conductor 42 is, in turn, covered with an encapsulant layer 44. Thus, Ovshinsky lacks any teaching or suggestion that a contact pad, let alone a contact pad that includes the features recited in independent claim 12, may contact any of the memory elements thereof. The teachings of Buiguez are limited to silicon-containing photoresists that are useful for forming photomasks. Therefore, it is respectfully submitted that independent claim 12 is allowable over the combination of Ovshinsky, Brown, and Buiguez.

Claims 13-19 are each allowable, among other reasons, as depending from claim 12, which is allowable.

Independent claim 39 is drawn to an electrically erasable programmable memory device that includes, among other things, a memory element and a contact. The memory element includes at least one of an electrode and a memory cell that comprises a phase change material. The contact includes, among other things, an intermediate conductive layer positioned adjacent to

and in electrical and thermal communication with the memory element, as well as an insulator component adjacent the intermediate conductive layer.

Ovshinsky, Brown, and Buiguez each lack any teaching or suggestion of an electrically erasable programmable memory device that includes a memory element with an intermediate conductive layer of a contact positioned adjacent thereto and in electrical and thermal communication therewith. Rather, Brown teaches a contact pad that is located adjacent to a bond pad. The teachings of Ovshinsky are limited to a use of an upper conductor 42 that is encapsulated by an encapsulant layer 44 and that bridges adjacent memory elements. Ovshinsky lacks any teaching or suggestion that any of the memory elements may be contacted by a contact, let alone a contact that includes the features recited in independent claim 39. Buiguez merely teaches silicon-containing photoresists that may be used to form photomasks. Therefore, it is respectfully submitted that independent claim 39 is allowable over the combination of Ovshinsky, Brown, and Buiguez.

Claims 40-44 are each allowable, among other reasons, as depending from claim 39, which is allowable.

The subject matter to which independent claim 45 is directed is a semiconductor device that includes at least one contact with, among other things, an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with a structure of the semiconductor device that comprises a phase change component.

None of Ovshinsky, Brown, and Buiguez, taken alone or in combination, teaches or suggests a semiconductor device with a contact that includes an intermediate conductive layer

positioned adjacent to and in electrical and thermal communication with a structure of the semiconductor device that comprises a phase change component. Again, the contact of Brown is disposed against an underlying bond pad or conductive trace, while Ovshinsky teaches a device with memory elements that have an upper conductor 42 adjacent thereto and the teachings of Buiguez are limited to silicon-containing photoresists. Therefore, it is respectfully submitted that claim 45, as proposed to be amended, is allowable over the combination of Ovshinsky, Brown, and Buiguez.

Claims 46-54 are each allowable, among other reasons, as depending from claim 45, which is allowable.

Independent claim 56 recites an enhanced electrically erasable programmable element with a contact that includes "an intermediate conductive layer positioned adjacent to and in electrical communication with the electrically erasable programmable element; an insulator component disposed adjacent said intermediate conductive layer and over the electrically erasable programmable element so as to insulate same; and an electrically conductive contact layer adjacent said insulator component."

None of Ovshinsky, Brown, or Buiguez teaches or suggests an enhanced electrically erasable programmable element with a contact that includes an intermediate conductive layer positioned adjacent thereto and in electrical communication therewith. Moreover, none of Ovshinsky, Brown, or Buiguez teaches or suggests a contact that includes an insulator component and which is positioned over an electrically erasable programmable element so as to

insulate the programmable element. Therefore, it is respectfully submitted that independent claim 56 is allowable over the combination of Ovshinsky, Brown, and Buiguez.

Claims 57-66 are each allowable, among other reasons, as depending from claim 56, which is allowable.

Claim 69 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 71 is allowable, among other reasons, as depending from claim 32, which is allowable.

For these foregoing reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claims 7, 12-19, 39-54, 56-66, 69, and 71 are allowable over the combination of Ovshinsky, Brown, and Buiguez and, thus, that these references do not support a *prima facie* case of obviousness against any of claims 7, 12-19, 39-54, 56-66, 69, or 71.

It is, therefore, respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 7, 12-19, 39-54, 56-66, 69, and 71 be reversed.

(iv) Ovshinsky, Brown, Buiguez and Whitten

Claims 20, 55, and 67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ovshinsky, in view of Brown and Buiguez and, further, in view of Whitten.

Claim 20 is allowable, among other reasons, as depending from claim 12, which is allowable.

Claim 55 is allowable, among other reasons, as depending from claim 45, which is allowable.

Claim 67 is allowable, among other reasons, as depending from claim 56, which is allowable.

It is further submitted that each of claims 20, 55, and 67 is allowable because Whitten does not remedy the aforementioned deficiencies of Ovshinsky, Brown, Buiguez and the generally-available knowledge in the art with respect to the elements of independent claims 12, 45, and 56, respectively, that are lacking in Ovshinsky, Brown, and Buiguez, as well as with respect to providing one of ordinary skill in the art with some motivation to combine the teachings of Ovshinsky, Brown, and Buiguez in the manner that has been asserted.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 7, 11-20, 39-67, 69, and 71 be reversed.

(9) APPENDICES

A copy of claims 1-20 and 32-71 as presently amended is appended hereto as the "Appendix."

(10) CONCLUSION

It is respectfully submitted that, under 35 U.S.C. § 103(a):

(A) Claims 1-6, 8-10, 32-38, and 68-70 are nonobvious and, thus, allowable over the combination of teachings from Brown, in view of the teachings of Buiguez;

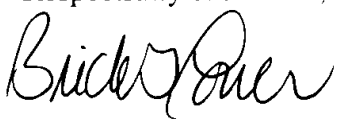
(B) Claim 11 is nonobvious and, thus, allowable over the teachings of Brown, in view of the teachings of Buiguez and, further, in view of teachings from Whitten;

(C) Claims 7, 12-19, 39-54, 56-66, 69, and 71 are nonobvious and, thus, allowable over the teachings of Ovshinsky, in view of the teachings of Brown and Buiguez; and

(D) Claims 20, 55, and 67 are nonobvious and, thus, allowable over the combined teachings of Ovshinsky, Brown, Buiguez, and Whitten.

It is, therefore, respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-20 and 32-71 be reversed and that each of these claims be allowed.

Respectfully submitted,



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APPENDIX

CLAIMS

1. (Amended four times) A contact for a semiconductor device, comprising:

an intermediate conductive layer contacting and in electrical communication with a structure located at a lower level than a silicon-containing dielectric layer of the semiconductor device;

an insulator component positioned adjacent said intermediate conductive layer so as to at least thermally insulate said structure; and

an electrically conductive contact layer adjacent said insulator component and in communication with said intermediate conductive layer.

2. (original) The contact of claim 1, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

3. (original) The contact of claim 1, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

4. (Amended) The contact of claim 1, wherein said insulator component comprises an insulator material including at least one of undoped silicon dioxide, doped silicon dioxide, silicon nitride, a thermoset polymer, and a thermoplastic polymer.

5. (original) The contact of claim 1, wherein said intermediate conductive layer comprises an electrically conductive material.

6. (original) The contact of claim 1, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

7. (Amended twice) The contact of claim 69, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature required to switch a phase change component in electrical communication with the contact between a plurality of states.

8. (Amended) The contact of claim 1, wherein said intermediate conductive layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

9. (original) The contact of claim 1, wherein said contact layer has a thickness of about 200 angstroms or less.

10. (original) The contact of claim 1, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature required to switch a phase change component in electrical communication with the contact between a plurality of states.

11. (Amended) The contact of claim 1, wherein said contact layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

12. (Amended three times) A contact for a memory element of a semiconductor device, the memory element including a phase change component, the contact comprising:
an insulator component comprising a thermally and electrically insulative material;
an intermediate conductive layer adjacent said insulator component and contacting and in electrical and thermal communication with the memory element; and
a contact layer adjacent said insulator component and in electrical contact with said intermediate conductive layer, said contact layer and said intermediate conductive layer substantially enveloping said insulator component.

13. (Amended) The contact of claim 12, wherein said thermally and electrically insulative material comprises at least one of undoped silicon dioxide, doped silicon dioxide, silicon nitride, a thermoset resin, and a thermoplastic polymer.

14. (original) The contact of claim 12, wherein said intermediate conductive layer comprises an electrically conductive material.

15. (original) The contact of claim 12, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

16. (original) The contact of claim 12, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of the phase change component from a first state to a second state.

17. (Amended) The contact of claim 12, wherein said intermediate conductive layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

18. (original) The contact of claim 12, wherein said contact layer has a thickness of about 200 angstroms or less.

19. (original) The contact of claim 12, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of the phase change component from a first state to a second state.

20. (Amended) The contact of claim 12, wherein said contact layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

32. (Amended four times) A contact for a semiconductor device including a contact layer and an intermediate conductive layer which partially contact one another and substantially envelop an insulator component, the contact contacting a structure located at a lower level than a

silicon-containing dielectric layer of the semiconductor device so as to at least thermally insulate the structure, the contact fabricated by the process comprising:

forming the intermediate conductive layer on a surface of the semiconductor device and in electrical thermal communication with an active device region of the semiconductor device;

depositing a dielectric layer on the intermediate conductive layer;

patterning said dielectric layer to define the insulator component;

forming the contact layer substantially over an exposed area of the insulator component and in electrical communication with the intermediate conductive layer;

patterning the intermediate conductive layer; and

patterning the contact layer.

33. (Amended) The contact of claim 32, wherein said forming the intermediate conductive layer comprises disposing a conductive material in electrical and thermal communication with a phase change component of said active device region.

34. (original) The contact of claim 32, wherein said forming the intermediate conductive layer comprises forming a thermally conductive material layer having a thickness of about 200 angstroms or less.

35. (original) The contact of claim 32, wherein said forming the intermediate conductive layer comprises depositing a thermally conductive material.

36. (original) The contact of claim 32, wherein said patterning said dielectric layer comprises etching and employs the intermediate conductive layer as an etch stop.

37. (original) The contact of claim 32, wherein said forming the contact layer comprises forming an electrically conductive material layer having a thickness of about 200 angstroms or less.

38. (Amended) The contact of claim 32, wherein said forming the contact layer comprises depositing an electrically conductive material.

39. (Amended three times) An electrically erasable programmable memory device, comprising:

a memory element including an electrode adjacent a memory cell, at least one of said electrode and said memory cell comprising a phase change material; and

a contact including an intermediate conductive layer contacting and in electrical and thermal communication with said memory element, an insulator component adjacent said intermediate conductive layer, and a contact layer adjacent said insulator component and in electrical communication with said intermediate conductive layer.

40. (Amended) The electrically erasable programmable memory device of claim 39, wherein said intermediate conductive layer contacts said electrode.

41. (Amended) The electrically erasable programmable memory device of claim 39, wherein said contact layer and said intermediate conductive layer substantially envelop said insulator component.

42. (Amended) The electrically erasable programmable memory device of claim 39, wherein said insulator component is sandwiched between said contact layer and said intermediate conductive layer.

43. (Amended) The electrically erasable programmable memory device of claim 39, wherein said contact layer has a thickness of about 200 angstroms or less.

44. (Amended) The electrically erasable programmable memory device of claim 39, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

45. (Amended three times) A semiconductor device including at least one contact, the at least one contact comprising:

an intermediate conductive layer contacting and in electrical and thermal communication with a structure of the semiconductor device comprising a phase change component;

an insulator component disposed adjacent said intermediate conductive layer; and

a contact layer adjacent said insulator component and in electrical communication with said intermediate conductive layer.

46. (original) The semiconductor device of claim 45, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

47. (original) The semiconductor device of claim 44, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

48. (original) The semiconductor device of claim 45, wherein said insulator component comprises a thermally insulative material.

49. (original) The semiconductor device of claim 45, wherein said intermediate conductive layer comprises an electrically conductive material.

50. (original) The semiconductor device of claim 45, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

51. (original) The semiconductor device of claim 45, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

52. (Amended) The semiconductor device of claim 45, wherein said intermediate conductive layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

53. (original) The semiconductor device of claim 45, wherein said contact layer has a thickness of about 200 angstroms or less.

54. (original) The semiconductor device of claim 45, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

55. (Amended) The semiconductor device of claim 45, wherein said contact layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

56. (Amended four times) An enhanced electrically erasable programmable element including a contact comprising:

an intermediate conductive layer contacting and in electrical communication with the electrically erasable programmable element;

an insulator component disposed adjacent said intermediate conductive layer and over the electrically erasable programmable element so as to insulate same; and

an electrically conductive contact layer adjacent said insulator component.

57. (original) The enhanced electrically erasable programmable element of claim 56, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

58. (original) The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

59. (original) The enhanced electrically erasable programmable element of claim 56, wherein said insulator component comprises a thermally insulative material.

60. (Amended) The enhanced electrically erasable programmable element of claim 56, wherein said insulator component comprises thermally insulative material including at least one of undoped silicon dioxide, doped silicon dioxide, silicon nitride, a thermoset resin, and a thermoplastic polymer.

61. (original) The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises an electrically conductive material.

62. (original) The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

63. (original) The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of electrical conductivity states.

64. (Amended) The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

65. (original) The enhanced electrically erasable programmable element of claim 56, wherein said contact layer has a thickness of about 200 angstroms or less.

66. (original) The enhanced electrically erasable programmable element of claim 56, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

67. (Amended) The enhanced electrically erasable programmable element of claim 56, wherein said contact layer comprises at least one of a refractory metal, a refractory metal nitride, and aluminum.

68. (Added and mended) The contact of claim 1, wherein at least one of said intermediate conductive layer and the electrically conductive contact layer abuts a major surface of said silicon-containing dielectric layer.

69. (Added) The contact of claim 1, wherein said structure comprises a phase change component.

70. (Added and amended) The contact of claim 32, wherein at least one of said intermediate conductive layer and said contact layer abuts a major surface of said silicon-containing dielectric layer.

71. (Added) The contact of claim 32, wherein said structure comprises a phase change component.